

# Computer Processors (PART-2)

## Performance

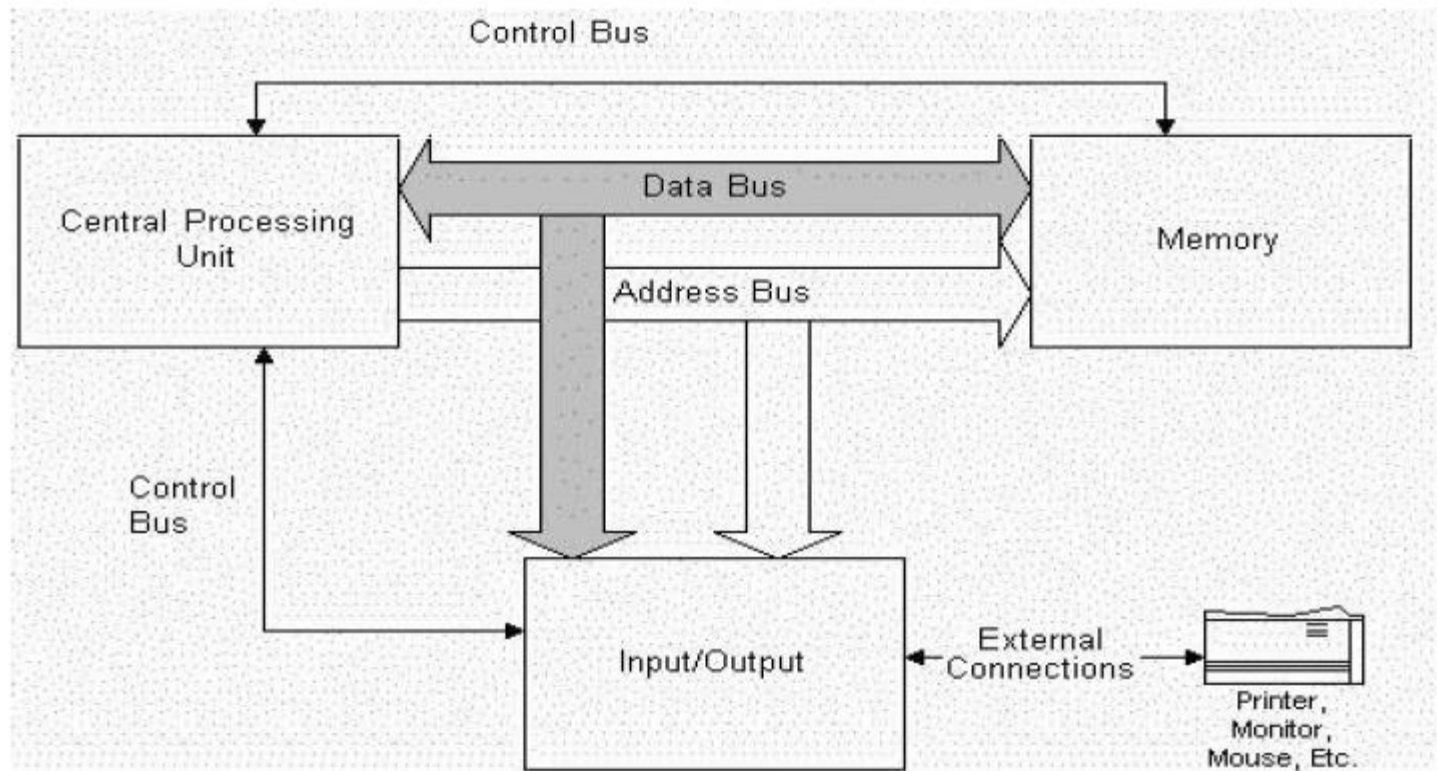
A decorative graphic consisting of several horizontal lines of varying lengths and colors (teal, light blue, white) extending from the right side of the slide towards the center.

# Performance Issues

- We want the CPU to be working as efficiently as possible
- We want to get data to and from the CPU as fast as possible

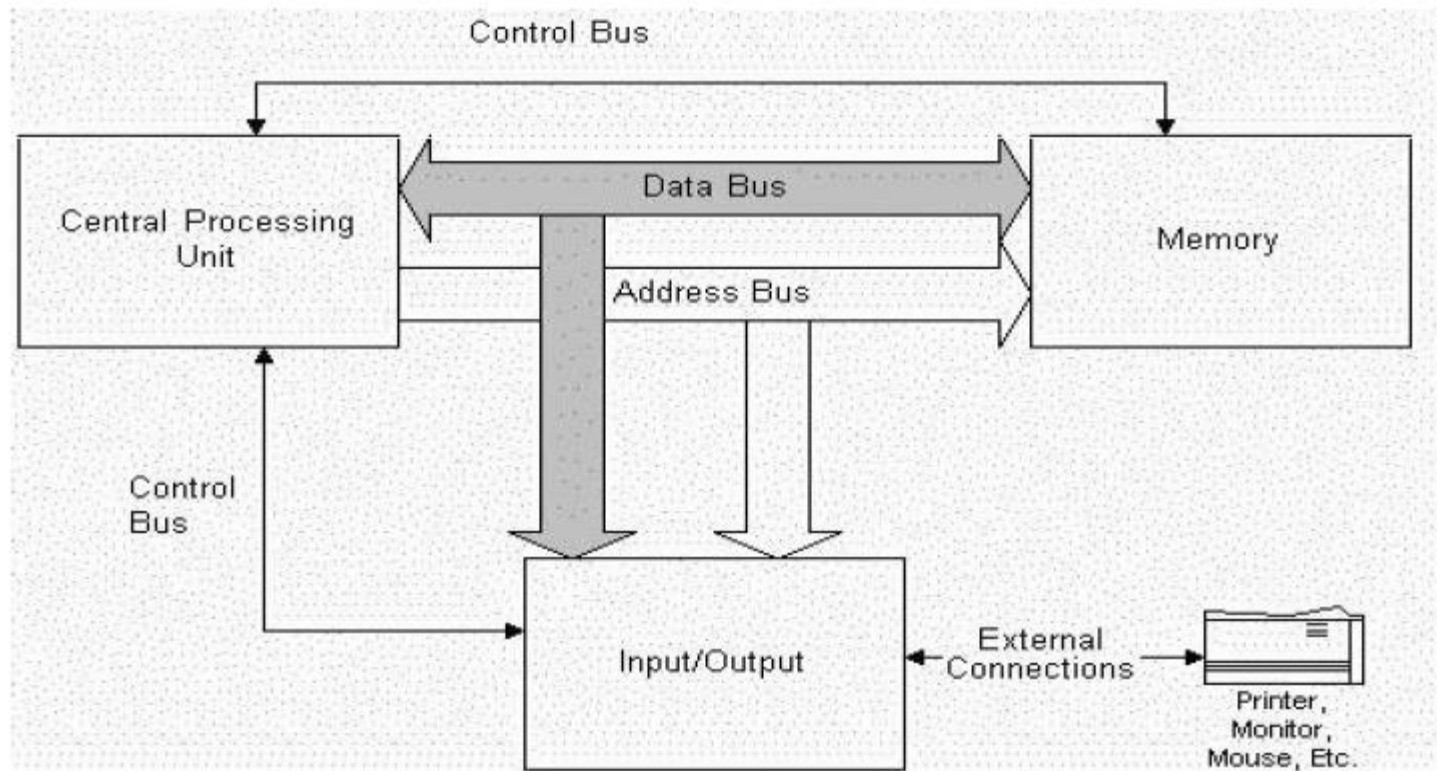
# Transferring data

- So far we have shown the CPU handling all data transfers



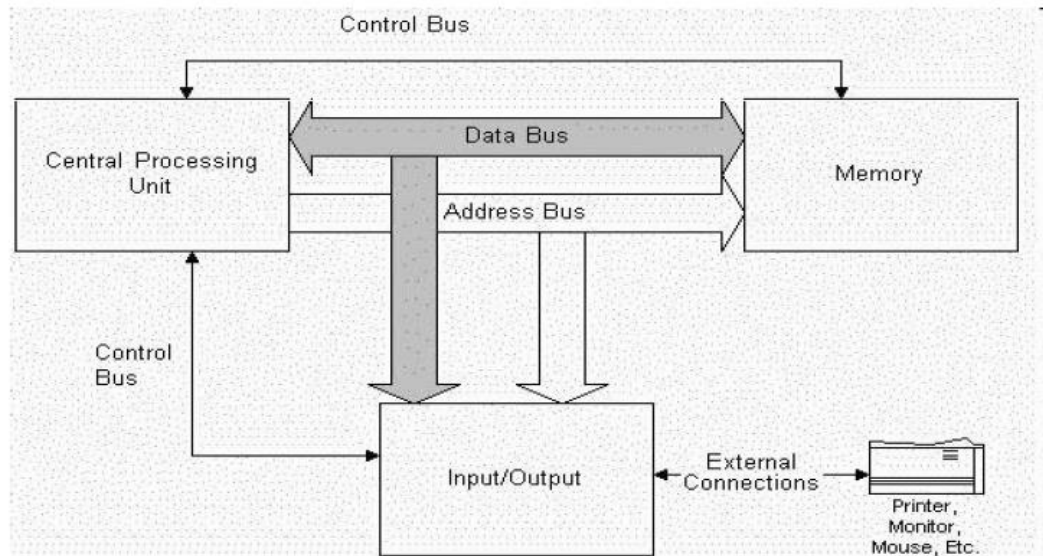
# Transferring data

- What is the sequence to read data into memory from an input device?



# Transferring data

- CPU puts input device address on data bus
  - CPU reads data into register from device using data bus
  - CPU puts memory address on address bus
  - CPU writes data from register to memory
- from register to memory



# DMA (Direct memory access)

- Transferring large amounts of data will use a lot of CPU time
- This overhead can be reduced using DMA
- Devices are fitted with their own controllers
- DMA controllers allow devices to transfer data without involving the CPU
  - Disk drives
  - Graphics cards
  - Sound cards
  - Network cards

# How DMA Works

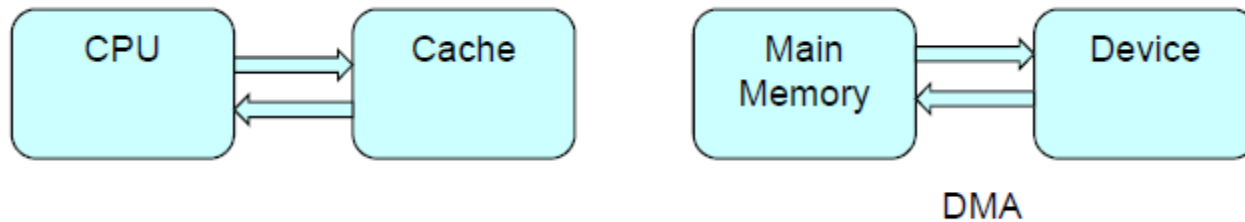
- The CPU will start a transfer by issuing a DMA read or write command to the device
- Must include the start address and the amount of data to be transferred
- The device takes control of the bus
  - Transfers the data directly
  - Raises an interrupt when it is complete

# How DMA Works

- The CPU can do other work when a DMA transfer occurs
- But if the DMA device has control of the address and data busses, what can the CPU work on?

# How DMA Works

- The CPU can work on data in the cache



# Memory Performance

- Factors affecting memory performance
  - Width of the address bus
  - Width of the data bus
  - Memory speed
  - Memory transfers per clock cycle

# SDR (single data rate RAM)

- Let us start our analysis with:
  - Bus speed = 133 MHz
  - Processor = 32 bit
  - Address bus = 32 bit
  - Data bus = 64 bit
- With SDR RAM
  - 64 bits are transferred each clock cycle
  - Transfer rate =  $64 \times 133 = 8512/8 = 1064$  MB/s

# DDR (double data rate RAM)

- With DDR RAM
  - 64 bits are transferred twice each clock cycle
  - $64 \times 133 \times 2 = 17024/8 = 2128 \text{ MB/s}$
- Double the theoretical performance of SDR

# DDR2

- With DDR 2 RAM
  - 64 bits are transferred four times each clock cycle
  - $64 \times 133 \times 4 = 34048/8 = 4256 \text{ MB/s}$
- Double the theoretical performance of DDR

# Dual channel DDR2

- Dual channel introduces a second memory controller and memory
- This effectively doubles the bus width to 128 bits
- With Dual channel DDR 2 RAM
  - 128 bits are transferred four times each clock cycle
  - $128 \times 133 \times 4 = 68096/8 = 8512 \text{ MB/s}$

# Increasing the bus speed

- If the bus speed is changed to 400 MHz with Dual channel DDR 2 RAM
  - 128 bits are transferred four times each clock cycle
  - $128 \times 400 \times 4 = 204800/8 = 25600 \text{ MB/s}$

# Task due Next Class

- What speeds can DDR3 reach?

# Processor's Pipeline

- A whole task that has been broken out into smaller sub-tasks.
- Concept actually has its roots in mass production manufacturing plants
- By taking several steps that a CPU needs to do execute a single instruction and overlaps them, so the computer is running those steps in parallel.

# Processor's Pipeline



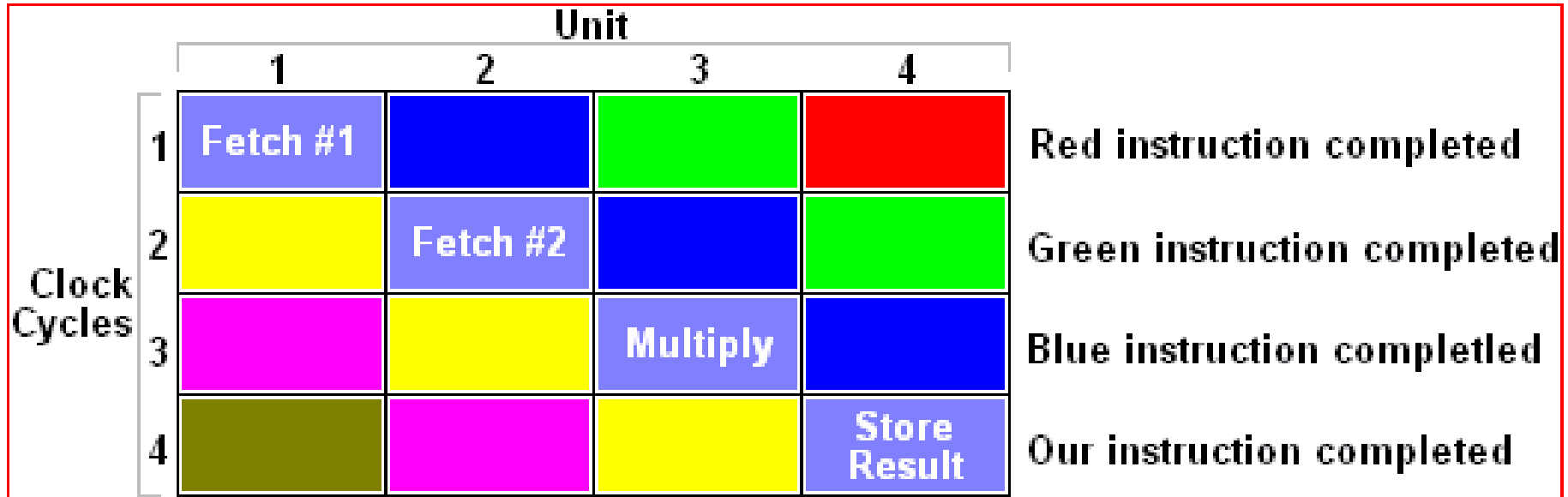
# Processor's Pipeline



# Processor's Pipeline



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# Processor's Pipeline

